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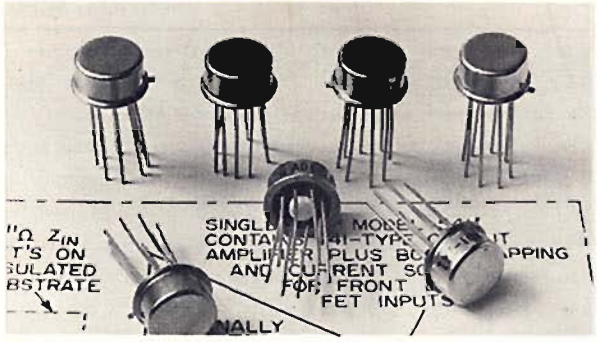
High Performance IC Fet-Input Op Amp

by Douglas R. Sullivan and Modesto A. Maidique

Ever since the introduction of the first IC operational amplifier, users have felt the need for a FET-input amplifier having performance comparable to that of the best discretes, but with the reliability, low cost, and small size inherent in IC technology. With such an amplifier, one could realize the usual applications in low-voltage and current measurements at high impedance, and high-accuracy integration, differentiation, and sample-hold. In addition, it would open up new areas of application in military, aerospace, medical, scientific, and remote probe equipment. Such an amplifier is now a practical reality, the AD503L. The authors discuss the design and process techniques that have made it feasible.



IN THIS ISSUE

For the first time in a TO-99 hermetically-sealed package: A commercially available FET-input operational amplifier with 5pA bias current, "zero" offset voltage, 5V/μs slew rate, same pin configuration and output characteristics as the popular AD741, and all at reasonable cost. Behind AD503L's success: Two happily-married chips, automatic laser trimming, clever circuit design, and Analog's Fourth Generation IC production facility.

INTRODUCTION

The AD503L, a 5pA bias current and "zero" offset voltage FET input operational amplifier, has been realized by combining in a TO-99 package (same pin configuration as 741 types[1]) monolithic chips and a thin film resistor network, as shown in Figure 1. The two monolithic devices consist of a dual FET chip and a modified "741 type" operational amplifier. The two chip approach was chosen over the single chip technique (where the FETs are integrated with the bipolar op amp) to permit independent optimization of both chips. By manufacturing the FET and bipolar devices separately, the processing steps can be tailored to achieve the highest performance without compromise.

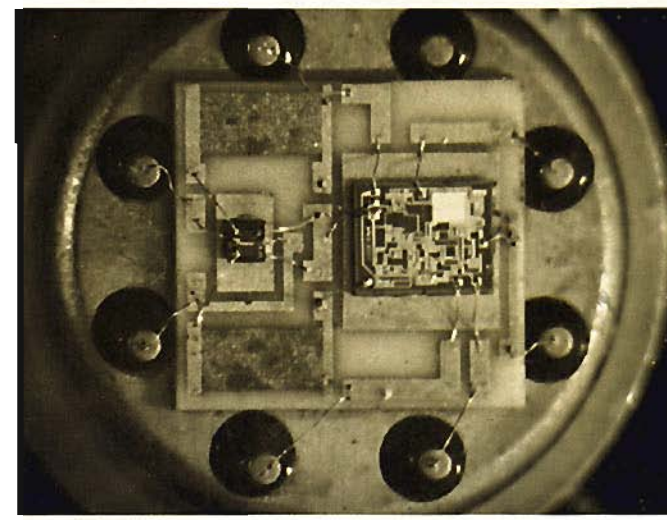


Figure 1. Model AD503L FET-Input IC Op Amp

The two-chip approach can be used to produce, with near-100% yield, *and therefore attractively low price*, an amplifier with input currents of less than 5pA. However, such an amplifier will still have a relatively high offset voltage. In order to reduce the offset voltage while retaining minimum offset voltage drift, the offset voltage must be nulled at the FET source terminals. This is accomplished by *active trimming* of the thin film source resistor network with an automatic tape-controlled, Q-switched YAG laser system. Typical performance for the AD503L circuit is tabulated in Figure 2.

Parameter	Model 503J	Model 503K	Model 503L	Units
Open-loop Gain (de rated load)	50,000	50,000	50,000	V/V
Rated Output Voltage, min (R_L = 2kΩ)	±10	±10	±10	V
Current, min	5	5	5	mA
Frequency Response				
Unity Gain, Small Signal	1	1	1	MHz
Full Power	100	100	100	kHz
Slew Rate (Unity Gain) min	6	6	6	V/μs
Input Offset Voltage				
Initial Offset	20	8	0.5	mV
Avg vs. Temp (0°C to +70°C)	30	15	15	μV/°C
vs. Supply Voltage	300	200	200	μV/V
Input Bias Current				
Initial bias, +25°C (doubles per 10°C)	15	5	5	pA
Offset Current	5	2	2	pA
Input Noise (50kHz bandwidth)	8	8	8	μV rms
Input Voltage Range				
Common mode Voltage, min	±10	±10	±10	V
Common Mode Rejection	80	80	90	dB
Power Supply				
Voltage, rated Specifications	±15	±15	±15	V
Current, Quiescent	4.5	4.5	4.5	mA

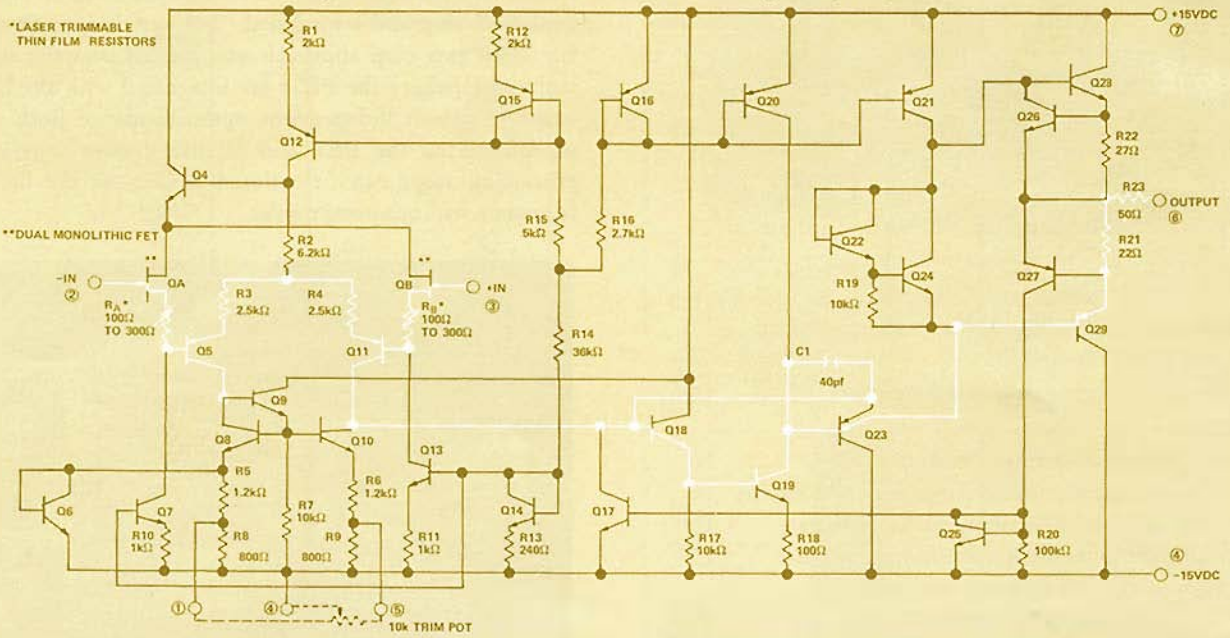
Figure 2. Typical characteristics of Model 503L and two untrimmed versions (costing somewhat less)

CIRCUIT DESCRIPTION

The AD503L is basically a two stage amplifier. As shown in the circuit diagram of Figure 3, the monolithic FET input pair is biased by current sources Q7 and Q13 to achieve ultra low input current performance combined with good thermal tracking. Bootstrapping of the FETs via Q4 results in a common mode rejection ratio of 80dB and constant input bias current over the ±10V common mode range. Due to the close matching of output impedance of the paired monolithic FETs, the use of bootstrapping improves the CMRR of the amplifier only moderately. However, this feature is included to make the bipolar integrated circuit chip flexible enough to provide excellent CMRR even if used with separate matched FET chips.

The FET drain-to-source operating voltage is determined by the voltage across the R2, R3, R4 resistor network and is set at 1.5V to maximize the common mode range. The ±10V

Figure 3. Schematic of the AD503L FET-Input Op Amp



Highlighted lines indicate signal flow path through the amplifier for negative output voltages. (To preserve simplicity, only half of the signal path through the differential to single ended converter, Q8, Q9, Q10, is shown).

C1, as in the 741, serves as a Miller integrating capacitor across Q19 to ensure that the response of the amplifier is dominated by a single time constant, thus providing unconditional dynamic stability with resistive feedback for any loop gain. Slew rate is, nevertheless, an order of magnitude higher than that of ordinary 741 types because of the increased collector current in Q5 and Q11. The tenfold increase in collector current is not reflected to the input since the pnp diff amp pair (Q5, Q11) is buffered to 5pA input current by the monolithic FET pair QA and QB.

common mode range requires the use of FETs with gate-to-source voltage of less than 2V at the operating current of 200μA. Resistors R3 and R4 also supply emitter degeneration, and therefore gain control, for the Q5, Q11 gain stage. Reduction of the gain of the Q5, Q11 pair is necessary to insure adequate stability with a single 40pF monolithic internal capacitor, while maintaining an operating current for Q5 and Q11 of 100μA (which is an order of magnitude higher than the collector current of an AD741 first stage). This increase in operating current results in an order of magnitude improvement in slew rate (6V/μs—see Figure 4) over that of the AD741. The only disadvantage of this approach is the possibility of increased offset voltage and offset voltage drift due to mismatch between R3 and R4. However, these effects are minimized by careful layout and good processing.

Transistors Q8 and Q10 serve as active loads for the first gain stage; the resistors, R5, R8, R6 and R9 set the emitter currents and allow for low impedance external offset nulling.

Q6 clamps the emitter of Q8 and prevents the base of Q8 from rising above the collector of Q10 when large currents are caused to flow through Q5. Thus Q6 prevents Q10 from saturating, eliminating a possible latch up mode.

The main bias chain for the amplifier consists of Q14, Q15, Q16, R12, R13, R14, R15 and R16. Here, diode-connected Q14 supplies the reference voltage for the input current sources, Q7 and Q13, while diode-connected Q15 supplies a reference voltage for Q12, the first gain stage current source; and Q16 provides a reference potential for the output section of the amplifier. Q15 and Q16 operate independently to decouple the output voltage from the input stage when Q21 goes into saturation.

The circuitry that follows the first gain stage: the integrating second stage (Q18, Q19) and the output followers (Q23, Q28 and Q29) are almost identical to those of the AD741 circuit presently in usage today. However, it should be noted that this part of the circuit still does not correspond to the published 741 diagrams.[2,3] The basic differences are twofold. First, the collector of Q18 has been connected to the V+ line to increase the load impedance at the collector of Q10. Second, an additional buffer stage Q21, Q23 has been added to the "old style" circuit to obtain higher voltage gain and lower output impedance and reduce the requirements on the output PNP beta. A second emitter was added to Q23 to divert Q18's base current under overload conditions and thus prevent Q19 from going into saturation and increasing the current drawn by Q18. As can be concluded from study of the diagram, the amplifier has both positive and negative current limiting as well as input overvoltage protection against supply voltage levels of either polarity.

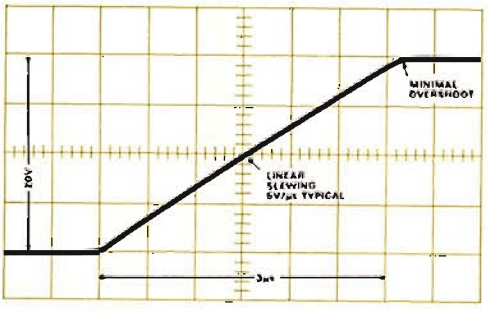


Figure 4. Slewing Characteristics

CONCLUSIONS

The excellent input characteristics of the AD503L (Figure 2) indicate what can be accomplished with the combination of monolithic FET, monolithic bipolar, thin film and laser trim technologies. These characteristics, combined with moderately high slew rate, make the AD503L ideal for sample-and-hold and fast buffer applications. Other usage includes electrometer and photocell amplifiers as well as general high impedance applications. The results obtained with the approach that has been outlined point towards the future genesis of sophisticated linear microcircuits: a skillful blend of two or more technologies to obtain optimum device performance at reasonable cost.

[1] Data Sheet, AD741 Operational Amplifier
[2] Fullagar, D. "A New High Performance Monolithic Op Amp" Fairchild circuit description, 1968
[3] Maidique, M. A., Jewell, R. F., Sullivan, D. R., "Characterization and Analysis of a High Performance Op Amp Family" Transitron Application Brief, 1969

AUTHORS

Douglas R. Sullivan and Dr. M. A. "Mitch" Maidique have been significant contributors to Analog Devices' linear integrated circuit development program and were instrumental in the establishment of our IC production facility.

Doug Sullivan was an Assistant Director of the MIT Instrumentation Laboratory until 1966, when he left MIT to found the Linear IC group at Transistron. He was instrumental in the conception and development of the first Teradyne J263 Linear IC Test System, which was subsequently delivered to his group in late 1968. Since then, he has continued to pioneer improvements in linear IC test techniques. He holds both BS and MS degrees in electrical engineering from MIT. At present, he is President of Nova Devices, Inc.

"Mitch" Maidique taught courses in circuit theory and linear IC design at MIT and has consulted on linear IC design, testing, and evaluation. Mitch is the author of various publications on discrete and integrated circuit design. He holds four degrees from MIT, including a Ph. D. in solid state electronics. At present he is Vice President, Engineering at Nova Devices, Inc.

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Choosing and Using N-Channel Dual J-Fets

Monolithic dual FET's have made parameter matching obsolete—eliminating laborious sorting and grading. Their improved performance (e.g. 5μV/°C offset drift) and reduced cost make them a natural choice for many applications. But there are important differences in construction among dual J-FETs, which determine temperature coefficients, performance, reliability, and consequently, choice for a given application.

INTRODUCTION

The field-effect transistor is now a widely-accepted circuit component because of its high input impedance, low noise, and great versatility. It is used in amplifying, switching, modulating, and generating signals. FET's are used in pairs as differential input stages for dc amplifiers, because of their great advantages of picoampere-level input leakage currents and teraohm input impedances. However, these advantages have been to some extent counterbalanced by the difficulty of obtaining and using matched units to obtain high common-mode rejection and low offset voltage and drift.

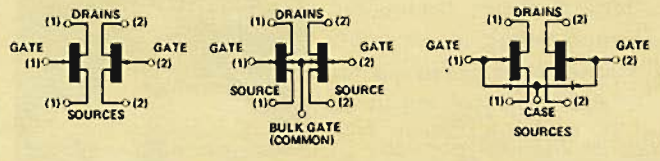
Recently, three types of high-performance matched pairs of junction FET's in single cans have become available. They are:

1. *Hybrids:* two chips that have been graded, selected, and mounted on a single header. (Example: Siliconix U235)
2. *Common-gate interdigitated:* single monolithic chips consisting of two FET's in intimate proximity with a common back side (bulk) gate. (Example: National FM1111)
3. *Monolithic isolated:* single monolithic chips containing two FET's electrically separated by diffused isolation diodes. (Example: Analog Devices AD3954)

In this article, we shall compare the differences in construction techniques, key specifications, and application philosophy among the three types, and show details of several applications employing monolithic isolated dual FET's. In addition, we shall tabulate the salient specs of two contrasting families of monolithic diffusion-isolated dual FET's: the AD3954A–8 general purpose duals and AD5902–9 ultra-low leakage small-geometry duals.

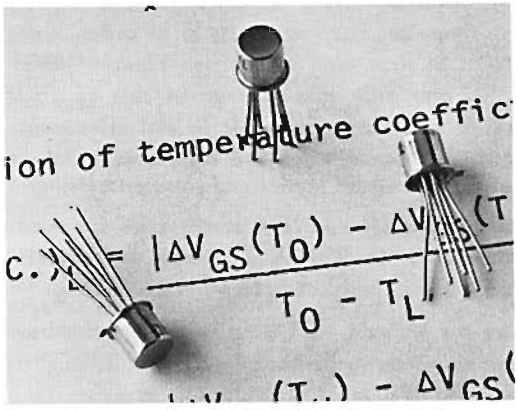
WHY A DUAL FET?

Dual FET's are used primarily in applications calling for two identical FET's. However, if they can be produced cheaply enough, (and they can—the monolithic AD3958, in the hermetic package, is cheaper than a pair of discrete FET's in plastic packages) they may also be considered in applications for a pair of independent (but similar) FET's, where space and cost can be saved by using two devices in the same can—if interaction of the elements of the dual device does not raise new problems.



(a) Hybrid Types *(b) Monolithic Common-Gate Types* *(c) Monolithic Junction-Isolated Types*

Figure 1. Dual-FET Schematic Diagrams



The bulk of applications for identical FET's are in the input stages of high-impedance operational amplifiers and comparators, where stability with temperature and common mode rejection depend greatly on parameter match. Applications for more-than-one FET include squarers, adjustable-frequency filters, switches, series-shunt voltage-variable attenuators, current sources, etc. Specific examples of some of these applications will be discussed at length in this article.

HOW ARE DUAL FETS MADE? WHAT ARE THE ADVANTAGES AND DISADVANTAGES?

Hybrids are made by collecting relevant data on a large number of individual FET chips, then, with the aid of a computer, selecting pairs that match to a specified degree. These are then mounted on a header that has two insulated mounting pads. To maintain the expense and yields within reason, the matching is usually performed at only one operating point (the nominal zero-drift drain current, I_{DZ}. As will be shown below, this may ensure excellent (though often nonlinear) temperature characteristics under one set of operating conditions; but detailed differences in linearity between one device and another may make the matching fruitless if the device is to be operated at a different value of drain current.

In addition, the dual-chip assembly is sensitive to thermal gradients, and will thus have greater than desired drift, due to the following: overloads; ambient temperature transients; static thermal gradients developed by adjacent circuitry.

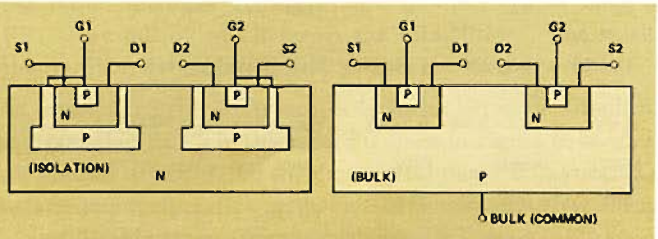
Furthermore, the handling that is inherent in measuring, storing, finding, and assembling pairs of chips has three disadvantages: it is more costly than handling single chips, it inevitably results in some loss of yield between measurement and assembly (causing a further increase in cost); and it tends to reduce ultimate reliability. The dual-chip FET does have the advantage of virtually complete *electrical* independence of the two FET's.

Monolithic duals are built in two ways, as shown in Figure 2. In both cases, the drain-source channel runs between an upper

gate terminal and a lower "bulk" gate. In some *interdigitated* duals, the bulk gate is common to both FET's and brought out to a separate terminal; in the *isolated* duals, two series-opposing diodes separate the bulk gates of the two FET's, and the bulk gates are internally connected to the top gates. Both types overcome the disadvantages of hybrid duals. Identification of chips containing matched pairs occurs at the wafer stage, and no extra handling of chips is required. Not only do the units that match have excellent temperature tracking at the specified value of drain current, but because they are even more alike than "two peas in a pod," they track well at other current levels as well. (See Figures 4 and 5) In addition, the gate-source difference voltage vs. temperature is quite linear, which allows further improvement of temperature coefficient by external manipulations in some circuit applications, as will be discussed in the Applications section.

Isolated vs. Common-gate duals. Isolated dual FET's, such as Analog's AD3954, are grown side-by-side with bulk N material separating the two P back gates. This produces isolation by two diodes in series opposing, with better than ±40V gate-to-gate breakdown voltage. Thus, the two FET's can be operated independently, the same as the two-chip duals, at any levels within the 40V BV_{GSS} rating, with negligible interaction.

In the case of the interdigitated duals (e.g., FM3954), with a common back gate, when pinchoff voltage (1.0 to 4.5V) is exceeded, the depletion layer reaches the bulk, and a "reach-through" or "punch-through" phenomenon occurs, characterized by a sharp reduction in input impedance (analogous to zener breakdown). For some applications, the common bulk is not a serious weakness; there are even a few applications in which it is a positive advantage. For most applications, however, the prospect of interaction is at best a nuisance that the engineer must consider—and perhaps expend extra components to avoid or mitigate; at worst, it is a potential source of component failure, if the "punch-through" current rating (typically 100μA) is exceeded. Nevertheless, because of the "interdigitated" construction, in which both FET's share the chip area more intimately, these types are likely more closely to approach identity between the twins, particularly in room temperature match of V_{GS}.



(a) Isolated dual FET AD3954 (b) Common-Gate dual FET

Figure 2. Monolithic Dual FET Construction

MONOLITHIC VS. HYBRID DUALS:
Offset Voltage and Drift Considerations

Matched pairs are used primarily to minimize drift in op amps and comparators. Let us therefore consider the relative ability of monolithic and hybrid duals to cancel drift. Typical op amp circuits in which they are used will be found on pages 7 and 8.

With a given value of drain-source voltage applied to a single FET, the gate-to-source voltage is a function of drain current and temperature. If I_D is varied, the temperature coefficient of V_{GS} variation will also be found to vary in nonlinear fashion. In the example shown in Figure 3, it is 2.7mV/°C at I_D = 1mA, and very nearly zero at I_D = 200μA. FET's having this geometry

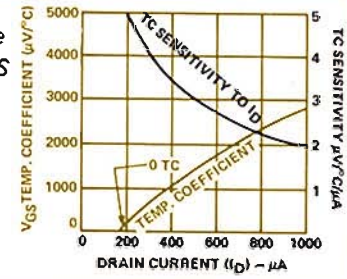


Figure 3. V_{GS} Temperature Coefficient (color) and V_{GS} TC Sensitivity (black) vs. Drain Current for single device (½ AD3954). (V_{DS} = 20V, I_{DSS} = 2mA)

are usually operated at currents near 200μA to take advantage of the small TC in that region. If the TC is low for single units, then matched pairs should have excellent performance. However, it is important to consider the rate of variation of TC with drain current, also plotted in Figure 3. For the example shown, it is about 4.5μV/°C per μA of I_D at I_D = 200μA. This means that for a 1% variation in I_D (viz., 2μA) the TC will change by about 9μV/°C.

If the FET's in a matched pair are not exactly alike, small local differences in shape of the V_{GS} TC curves will cause the offset vs. temperature to be nonlinear. In Figure 4, differential V_{GS} offsets are plotted vs. temperature for a monolithic dual FET and for a hybrid two-chip pair. It can be seen that the close identity of the FET's on the monolithic chip produces quite linear offset, which—because of its linearity—can be trimmed to "a gnat's eyebrow" by adjusting one of the drain currents. In the case of the two-chip device, while it meets the 10μV/°C specification on a gross basis, the nonlinearity precludes the possibility of further minimization of TC, except over a narrow range of temperatures.

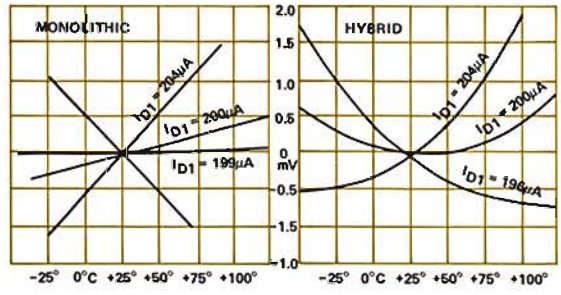


Figure 4. V_{GS1-2} differential offset voltage as a function of temperature for typical monolithic and two-chip hybrid dual FET's, under identical conditions. (Both are "10μV/°C" units.) V_{DG} = 20V, I_{D2} is initially set to 200μA, and the vertical scale represents departure from 25°C initial offset (millivolts)

The differences are further accentuated when the FET's are operated at values of drain current that differ greatly from the nominal match point. In Figure 5, the drain current is 500μA. For the monolithic pair, a 1% change in one of the currents is sufficient to restore a quite low TC. In the case of the hybrid, it is evident that matching is quite lost.

COMPARABLE SMALL GEOMETRY DUAL FETS, Condensed Specifications

Parameter	Symbol	Isolated Dual Monolithics (Analog Devices) AD5909	Hybrids 2N5909	Conditions T_A = +25°C, unless otherwise noted
Drift vs. Temperature	$\left\|\frac{\Delta V_{GS_{1-2}}}{\Delta T}\right\|$ max	40μV/°C	40μV/°C	V_{DG} = 10V, I_D = 30μA, −55°C<T_A<+25°C<T_A<+125°C
Offset Voltage	$V_{GS_{1-2}}$	50mV	15mV	V_{DG} = 10V, I_D = 30μA
Gate Current	$-I_G$ max	1pA	1pA	V_{DG} = 10V, I_D = 30μA
Gate Current	$-I_G$ max @ +125°C	1nA	1nA	V_{DG} = 10V, I_D = 30μA, T_A = +125°C
Transconductance	g_{fs} min–max	50–150μ mhos	50–150μ mhos	V_{DG} = 10V, I_D = 30μA, 1kHz
Transconductance Mismatch	$\left\|\frac{g_{fs_{1-2}}}{g_{fs}}\right\|$ max	5%	5%	V_{DG} = 10V, I_D = 30μA, T_A = +125°C
Saturation Current	I_{DSS} min–max	0.03–0.5mA	0.03–0.5mA	V_{DS} = 10V, V_{GS} = 0
Saturation Mismatch	$\left\|\frac{I_{DSS_{1-2}}}{I_{DSS}}\right\|$	5%	5%	V_{DS} = 10V, V_{GS} = 0
Pinchoff Voltage	$-V_p$ or $-V_{GS}$(off) min–max	0.6–4.5V	0.6–4.5V	V_{DS} = 10V, I_D = 1nA
Source–Gate Voltage	$-V_{GS}$ max	4V	4V	V_{DG} = 10V, I_D = 30μA
Gate Voltage	V_{GSS} Dt max	40V	40V	
Drain Voltage	V_{DSO} Dt max	40V	40V	
Gate-Gate Breakdown	V_{GGO} min	40V	80V	
Price (100+) *		$5.95	$5.95	

COMPARABLE MEDIUM-GEOMETRY DUAL FETS, Condensed Comparative Specifications

		Analog Devices Isolated Dual Monolithic		National Semiconductor Interdigitated Dual Monolithic		Siliconix Hybrids		
PARAMETER	SYMBOL	AD3954A	AD3958	FM3954A	FM3958	2N5196	U235	CONDITIONS
								T_A = +25°C, unless noted
Drift vs. Temperature	$\left\|\frac{\Delta V_{GS_{1-2}}}{\Delta T}\right\|$ max	5μV/°C	100μV/°C	5μV/°C	100μV/°C	5μV/°C	100μV/°C	V_{DG} = 20V, I_D = 200μA, −55°C<T_A<+25°C, +25°C<T_A<+25°C
Offset Voltage	$\|V_{GS_{1-2}}\|$	25mV	50mV	5mV	25mV	5mV	25mV	V_{DG} = 20V, I_D = 200μA
Gate Current	$-I_G$ max	50pA	50pA	50pA	50pA	15pA	50pA	V_{DG} = 20V, I_D = 200μA
Gate Current	$-I_G$, max @ +125°C	250nA	250nA	250nA	250nA	15nA	250nA	V_{DG} = 20V, I_D = 200μA, T_A = +125°C
Transconductance	g_{fs}, min–max	1000–3000μ℧	1000–3000μ℧	1000–4000μ℧	1000–3000μ℧	1000–4000μ℧	1000–3000μ℧	V_{DS} = 20V, V_{GS} = 0, 1kH
Transconductance Mismatch	$\left\|\frac{g_{fs_{1-2}}}{g_{fs}}\right\|$	1%	1%	3%	15%	3%	15%	V_{DG} = 20V, I_D = 200μA
Saturation Current	I_{DSS}, min–max	0.5–5mA	0.5–5mA	0.5–5mA	0.5–5mA	0.7–7mA	0.5–5mA	V_{DG} = 20V, V_{GS} = 0
Saturation Mismatch	$\left\|\frac{I_{DSS_{1-2}}}{I_{DSS}}\right\|$	5%	5%	5%	5%	5%	5%	V_{DG} = 20V, V_{GS} = 0
Pinchoff Voltage	$-V_p$ or $-V_{GS}$ (off) min–max	1–4.5V	1–4.5V	1–4.5V	1–4.5V	0.7–4V	1–4.5V	V_{DS} = 20V, I_D = 1nA
Source-Gate Voltage	$-V_{GS}$ min–max	0.5–4V	0.5–4V	0.5V	4.0V	0.2–3.8V	0.5–4V	V_{DG} = 20V, I_D = 200μA
Gate Voltage	V_{GSS} Dt, max	40V	40V	50V	50V	50V	50V	Either V_{GS} or V_{GD}
Drain Voltage	V_{DSO} Dt, max	40V	40V	50V	50V	50V	50V	
Gate-Gate Breakdown	V_{GGO}, min	40V	40V	<2V_{GS}(off)	See text	>50V	>50V	I_G = 1nA, I_D = 0, I_S = 0
Price (100+)*		$9.70	$2.15	$10.30	$1.80	$17.50	$3.00	

*As of 6 October 1970 †D indicates an absolute maximum limit above which degradation or destruction may occur

NOTES ON TWO FAMILIES: AD3954A, etc., vs. AD5906, etc.

The AD3954A, and its ilk are characterized by moderate drain current, y_{fs}, and gate leakage (typically 200μA, 2,000μ℧, and 20pA, respectively). The corresponding parameters for the AD5906 family are an order of magnitude lower (typically 20μA, 100μ℧, and 0.8pA, respectively). Both families have comparable offset and drift specifications. The AD3954 family is designed for general-purpose FET applications where reasonably good voltage gain and reasonably low offset and bias current are desired. The AD5909, because of its extremely low leakage current, is designed for electrometer and high impedance circuit applications. It should be operated with current-source drain loads (to squeeze the utmost in gain from its low transconductance) and V_{DG} should be maintained at a low constant value, irrespective of common mode level, through "bootstrapping", to minimize bias current variation with common mode swing. Its can should be connected to a common mode "guard" potential, to minimize bias current contributed by leakage to the outside world. Because of its lower g_m, the 5909 family is less suitable for fast applications.

This dependence of TC match on I_D is particularly important when dual FET's are used in the input stages of op amps with simple resistive ancillary circuitry. Drain current can vary widely with common mode voltage (unless constant current sources and/or "bootstrapping" are used), which in turn can produce substantial changes of TC in circuits using paired chips, considerably less with monolithic FET's.

These measured results depict the differences between two *specific* devices, but they are representative of their species. Hybrids often have better +25°C offset specifications than monolithics. However, since these offsets can be adjusted out without significant penalty, the better linearity of monolithics keeps them as the preferred choice. (Figures 7 and 8)

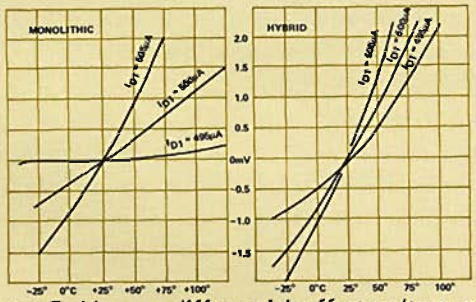


Figure 5. V_{GS1-2} differential offset voltage as a function of temperature for the same two FET's as in Figure 4, but with I_{D2} = 500µA. Same vertical scale as Figure 4.

Temperature Gradient

Another factor of importance when considering drift is the effect of unequal temperature changes in the two members of a matched pair. For the FET characterized in Figure 3, the TC at 200µA I_D is about 150µV/°C. Thus, under electrically balanced conditions, a 1°C thermal unbalance would cause a relative drift of 150µV. Such unbalances might be caused transiently if one of the FET's were momentarily cut off or saturated (as can happen quite easily in comparator applications). They might also be caused by a sudden change in the ambient temperature, with unequal heat flow to the two input transistors. They can even occur in the steady state if the FET's are in close proximity to a source of constant (or variable) heat flow (e.g., a load resistor). Then, the closer, the more identical, and the more intimately heat sunk the FET's are (all of which favors the monolithics), the smaller the transient variations and the shorter the recovery time.

An example of the difference in behavior between monolithic and two-chip FET's in this regard is given in Figure 6, in which are plotted offset vs. tab angle of typical dual FET's rotated in a stationary temperature gradient. The maximum offset change is considerably greater for the two-chip FET.

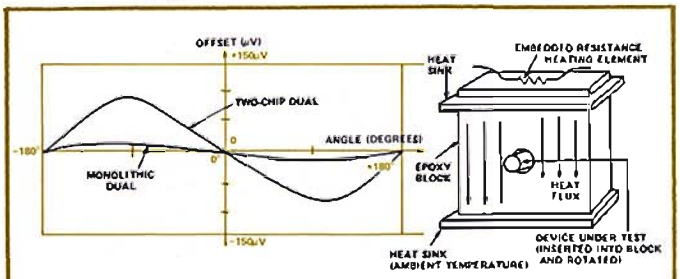


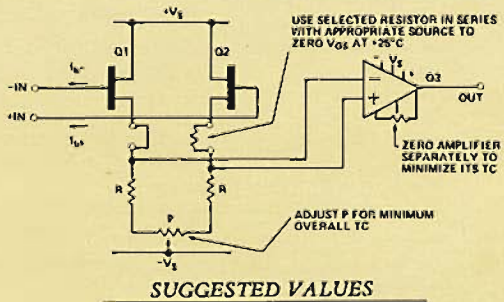
Figure 6. Offset Voltage vs. Angle of Can Tab to 1°C/mm Thermal Field

APPLICATION OF DUAL FETS

Operational Amplifiers (and Comparators)

This discussion will sidestep the controversy over whether to "make or buy" FET-input op amps. Such decisions depend on circuit complexity, budget, equipment/system requirements for performance, reliability, ease of manufacture, special features, and—the propensities of the project engineer and his management.* Suffice it to say that whether the decision is "make" or "buy", Analog Devices is always pleased to supply the active elements, be they complete FET-input op amps, or FET pairs with AD741 main amplifiers. The basic circuit applications discussed here utilize dual FET's, in conjunction with Analog's low-cost op amps, plus passive components.

FET input stage designs offer two basic options: FET's as source followers (essentially unity gain) or FET's as amplifiers. The circuits shown are by no means the most sophisticated designs available, but they are simple circuits that will perform reliably, provided that reasonable skill and care has been employed in laying out and wiring the circuits. All the rules that pertain to low-level high impedance circuitry apply here. For example, if a leakage path of as much as 10^{12} ohms exists between the +15V supply and the FET gates, input current will be increased by 15pA beyond the FET's own leakage current. This is marginal for 50pA applications and unacceptable for 1pA applications. To avoid excessive leakage, the high-impedance input leads should be guarded by (and the metal case connected to) a potential that is close to that of the input (common, in the case of inverters; the output, in the case of unity-gain followers; the feedback return—at low impedance—in the case of followers with gain).



SUGGESTED VALUES

I_B	Q1, Q2†	R*	P†	Q3†
50pA	AD3954A to AD3958	75kΩ	10kΩ AD79PR10k	AD741K
1pA	AD5906 to AD5909	500kΩ	50kΩ AD79PR50k	AD502K

*Resistors are 1% tolerance, low TC (15–100ppm/°C depending on allowable offset drift)
†Available from Analog Devices, Inc.

Figure 7. FET's Connected as Followers

Follower Circuit

Figure 7 shows a FET-input op amp using the dual FET's as followers. Use the table to determine circuit parameters and FET family, depending on the desired input "bias" current level. Choose the specific FET type as a function of desired voltage drift and offset level. Complete tabulations of specifications of available dual FET's, in both the AD3954A and AD5909 series are to be found in the family data sheets, available upon request. See page 6 for condensed specifications.

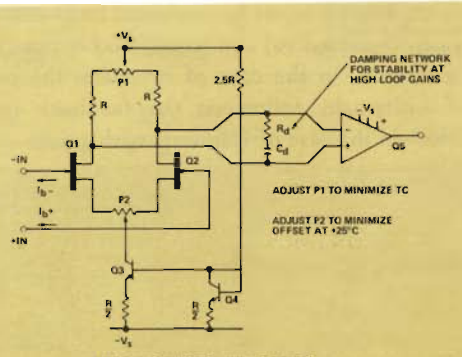
*However, the newly-announced AD503 (see page 1) is itself a compelling argument for "buy"

The resistors, R, can be 1% values, but they should have low temperature coefficients (preferably of the same polarity), from 15ppm/°C to 100ppm/°C, depending on the drift level desired and the FET pair used. Changes in resistor values affect the FET channel currents, and differential changes affect the offset drift temperature coefficient. Feedback maintains the voltages across the two resistors (and pot arms) very nearly equal, within the input error of the main amplifier.

The amplifiers specified for use with the FET's are low-drift types, because their drift adds directly to that of the FET's. The amplifier's own input offset (at the inputs of Q3) is first adjusted to zero, because minimum amplifier TC occurs near zero offset. Then potentiometer P is adjusted to minimize the variation of offset with ambient temperature. Finally a value of resistance empirically selected to minimize offset at +25°C is inserted in series with the appropriate FET source terminal.

Amplifier Circuit

The follower circuit has limitations: it does not reduce the influence of main amplifier offset; it does not reject variations in the negative supply voltage; the overall gain is only that of the main amplifier. On the other hand, it is capable of wide common mode swing, especially for positive values of CMV. The amplifier circuit in Figure 8 overcomes some of the limitations, at the cost of extra components and of reduced positive common mode swing (due to limitations imposed by the rated common mode range of the main amplifier).



SUGGESTED VALUES

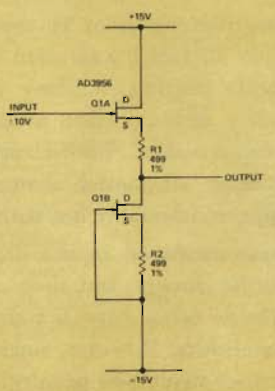
I_b	Q1, Q2†	R*	P1†	P2†	Q3, Q4†	Q5†	R_D	C_D
50pA	AD3954A to AD3958	25kΩ	2kΩ AD79PR2k	500Ω AD79PR1k	2N4880 Dual Transistor	AD741C	2.2kΩ	0.47μF
1pA	AD5906 to AD5909	150kΩ	10kΩ AD79PR10k	2kΩ AD79PR5k	2N4880 Dual Transistor	AD502J	15kΩ	0.05μF

*Resistors are 1% tolerance, low TC (15–100ppm/°C depending on allowable offset drift)
†Available from Analog Devices, Inc.

Figure 8. FET's Connected as Amplifiers

Here, the outputs from the FET preamplifier stage are taken from the drains. Q3 and Q4 and their associated resistors form a current source to maintain the total current drawn by Q1 and Q2 at a constant value little affected by common mode swing. Thus, this circuit will have better common mode rejection than the circuit of Figure 7, from −10V to +5V. It will also have better power supply rejection, and at least 20dB more gain at low frequencies. The additional gain supplied by the FET input stage reduces the effect of main amplifier offset and drift, allowing use of less costly amplifiers. To maintain stability at high values of loop gain, an RC damper between the inputs of Q5 (or feedback capacitance) is recommended. For best results, the resistors referred to R should be metal film types having low TC's, but the especially critical match of TC's (for lowest drift) is between the R's.

LOW DRIFT FOLLOWER

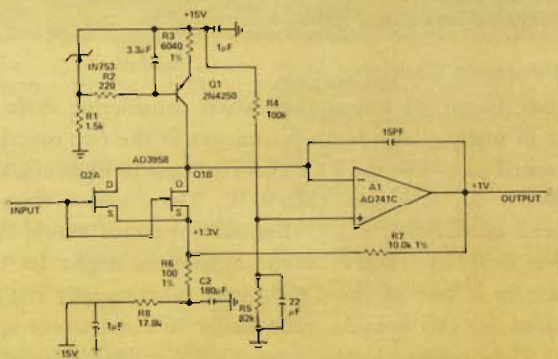


For applications where the FET is needed primarily to unload a very high impedance signal, this circuit may be used to buffer the input of a low cost op amp, such as the AD741C. It is an extremely simple outside-the-loop alternative to Figures 7 and 8.

As shown, it will be foolproof when driving loads of 100kΩ or higher, without any selection. FET's selected to have I_{DSS} of 1.5mA minimum can drive load resistances as low as 20kΩ, while maintaining linearity of 0.01% for a ±10V output range. At no load, the gain is typically 0.998. The output impedance is equal to $R_1 + 1/y_{fs}$.

To get the most out of the design, it is useful to choose the source resistors (R1 and R2) as a function of the load. The gate of Q1A should never be driven more positive than the source at the maximum positive input. R2 can be trimmed to zero the output. At no load (e.g., when driving a high-impedance op amp input—say, AD741C), short circuits may be substituted for R1 and R2.

LOW NOISE AC PREAMPLIFIER



This amplifier will provide a voltage gain of 100 over a bandwidth (−3dB) of 9Hz to 250kHz. It is well suited to such diverse sources as magnetic phonograph pickups (low impedance) and piezoelectric transducers (high impedance).

The AD3958 FET's provide an overall noise voltage of typically 1.1μV in a 50kHz bandwidth, referred to the input. (Noise current is also low, of the order of 1pA in the same bandwidth.) Paralleling the FET's increases the signal to noise ratio by 3dB, because transconductance increases directly with the number of units, while noise increases with the square root. In this circuit, each FET operates at a drain current of 0.5mA. However, if the units are selected for $I_{DSS} \geq 1$mA, voltage noise can be further reduced by about 2dB (25%) by reducing R3 to 3,010Ω and R8 to 9,090Ω, to increase drain current.

To make best use of the input stage's low noise, it must also have high gain, in order to minimize the noise contribution from the AD741C op amp. This is accomplished by using a current source (Q1) as the load in the drain circuit. The input signal should have a dc return path to ground for Q2's gate currents. This path can have an extremely high resistance (limited only by the need to avoid reverse-biasing the electrolytic capacitor C2) because of the AD3958's picoampere-level bias current.

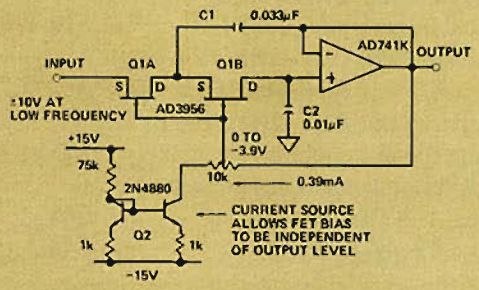
ADJUSTABLE LOW PASS FILTER

This circuit is useful primarily to filter out small ac noise components riding on a relatively slowly-varying signal. Gate voltage variation of matched channel resistances of the AD3956 allows adjustment of cutoff frequency over a 10:1 range (1:10kHz for the capacitance values shown) with 12dB/octave attenuation and 0.6dB peaking.

Signal or noise components in the vicinity of cutoff will suffer 3% harmonic distortion (at worst) just above ±150mV for 10kHz settings and ±15mV for 1kHz settings. Distortion will be proportionately less at lower frequencies, allowing larger signals to be passed. The reason for this is that the voltage drop across the FET resistors increases with frequency, but the drain voltage-drain current characteristic is linear only well below pinchoff. If FET's are selected for pinchoff at the higher end of the specified 1.0 to 4.5V range, linearity can be improved. If large ac signal components are present in the vicinity of cutoff, the input level should be reduced correspondingly.

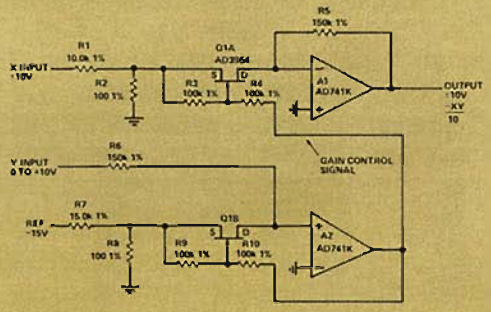
The cutoff frequency has a TC of about 1%/°C. The circuit should be fed from a low-impedance source, such as another operational amplifier.

Cutoff frequency ranges can be scaled directly by scaling the capacitance values. The 3.3:1 capacitance ratio provides 0.6dB corner peaking. Smaller ratios reduce peaking, larger ratios increase it. With 0.6dB peaking response is down about 1.2dB at the asymptotic cutoff frequency.



2 QUADRANT MULTIPLIER

This circuit is useful as a gain controller for ac or dc signals. A 0 to +10V Y input signal will control the gain of an X input signal in the ±10V range.



At Y = +10V, the gain is unity and typical best straight line linearity, when the X input is varied from −10V to +10V, is 0.1%. Nonlinearity increases as Y decreases to lower the gain. At a gain of 0.1, corresponding to Y = +1V, typical linearity is 1% and consists of mostly third harmonic distortion. Y input linearity is 1% from 1V to 10V.

The gain control portion of the system consists of Q1A which feeds an inverting operational amplifier A1. The FET is fed from a low source resistance made up of the divider R1 and R2 which delivers ±100mV to the source of Q1A. Normally, linearity, even at this signal level, is very poor as the bias on Q1A is raised towards the pinchoff voltage. By feeding some of the input signal back to the gate via R3, so as to maintain the gate signal voltage dynamically midway between the source and drain voltages, second harmonics are eliminated, leaving only third harmonics, and total distortion is greatly reduced. Distortion cancellation results from the excellent symmetry of the AD3954 which makes the source and drain essentially interchangeable and allows about a 5X larger input signal to be used for the same distortion, thus improving the signal to noise ratio.

For a gain range of 10 to 1, Q1A is operated as a variable resistance having a range from 1.5k to 15k. Since this varies the feedback ratio around amplifier A1, the −3dB bandwidth, which is typically 45kHz at a gain of 0.1, decreases to 4.5kHz at a gain of 1. The bandwidth can be readily increased by designing the circuit for lower input and output levels, say ±1V instead of ±10V, simply by reducing R1 and R5.

As a gain controller, only the upper portion of the circuit is needed; it is merely necessary to vary the dc input voltage to R4 in the range of −4V to 1. Zero gain occurs, of course, at the pinchoff voltage and the gain is somewhat temperature sensitive. Improved performance is obtained by the addition of the bias control circuit involving Q1B and operational amplifier A2. In this circuit, a dc reference voltage of +100mV derived from the 15V supply voltage is fed to the source of Q1B. Feedback automatically adjusts the resistance of Q1B to balance the current from the Y input through R6 so as to hold the positive input of A2 at virtual ground. This circuit then automatically produces a bias at the gate which varies in accordance with the characteristics of the particular FET and with temperature. This bias is the same as that required to produce the desired gain as a function of the Y input. By feeding the output of A2 to the bias resistor R4 for Q1A, the resistance of Q1A from source to drain can be made equal to the resistance of Q1B to the extent that the FET pair is matched. This circuit thus provides the correct gate bias and transforms the Y input voltage from −4V to 0 to the 0 to +10V range. If the FET's are perfectly matched, the gain of Q1A vs. temperature is compensated and nonlinearity vs. the Y input is also compensated. The circuit can be made to operate at different Y input voltage levels or at different reference voltages by changing R6 and R7. Note that the gain varies inversely with the supply voltage, which is used as a reference supply. Sensitivity can be decreased by using a reference zener diode.

There is a slight amount of feedthrough from the Y input when the X input is 0, which results in a small dc output proportional to the Y input if there is an offset in A1. This can be eliminated by balancing out the voltage offset of A1; in ac circuits it can be eliminated by inserting a large value tantalum coupling capacitor between the drain of Q1A and the negative input of A1.

NEW PRODUCTS

CHOPPER-STABILIZED OP AMP OFFERS 1μV/°C DRIFT FOR ONLY $33 (100+)

Model	233J	233K	233L
Gain, min (V/V)	10^7	10^7	10^7
Offset Drift, max (μV/°C)	1.0	0.3	0.1
Initial Offset, max (μV)	50	20	20
Bias Current, max (pA)	50	50	50
Bias vs. Temp (pA/°C max)	2	1	0.5
Rated Output, min (V,mA)	±10, 5	±10, 5	±10, 5
Voltage Noise, 0.01–1Hz (μV p-p)	1	1	1
5Hz–50kHz (μV rms)	3	3	3
Current Noise, 0.01–1Hz (pA p-p)	3	3	3
Unity Gain Bandwidth, min (kHz)	500	500	500
Full Power Bandwidth, min (kHz)	4	4	4
Price, 1–9 (U.S.$)	$45.	$54.	$75.
10–24 (U.S.$)	$40.	$49.	$68.

900 SERIES POWER SUPPLIES

Write for Free 4-Page Bulletin

NEW MODULAR POWER SUPPLIES FOR OP AMPS AND MICROLOGIC

In addition to the popular Models 902–904, Analog Devices now offers a complete new line of regulated short-circuit-protected power supplies in the "900" series. Dual supplies for op amps have voltages ranging from ±12V to ±24V and currents from 25mA to 1.0A, and prices start at $23. (1–9). Most of these supplies are encapsulated in the popular 2½" X 3½" X 0.88" "P" case.

Model	E_0(V)	I_0(mA)	$(1–9)	$(10–24)
907	±12	±25	23.	22.
909	±12	±50	49.	47.
908	±12	±100	59.	56.
915	±15	±25	23.	22.
904	±15	±50	39.	38.
902	±15	±100	49.	47.
916	±15	±300	98.	93.
917	±15	∓500	114.	108.
918	±15	±1000	148.	141.

Model	E_0(V)	I_0(mA)	$(1–9)	$(10–24)
931	±18	±25	23.	22.
935	±18	±50	55.	52.
932	±18	±100	65.	62.
933	±24	±50	55.	52.
934	±24	±100	65.	62.
906	5	250	39.	38.
903	5	500	49.	47.
905	5	1000	69.	66.

Available options include 205-240VAC primary (no extra charge), "crowbar" protection (standard on Models 903, 905), and interwinding shield.

LOW-DRIFT FET-INPUT INSTRUMENTATION AMPLIFIER FEATURES SINGLE RESISTOR GAIN SELECTION

Model 603L Characteristics	
Gain (G) (selected by single resistor)	$10^5/R_g$
Gain Linearity	0.1%
Gain Error (max)	3%
Output Drift (max)	5 (10+G)μV/°C
Bias Current (max)	20pA
Bandwidth, −3dB	1MHz/G
Common Mode Voltage	±10V
Common Mode Rejection	80dB
Price (1–9)	$95.

FAST-SETTLING OP AMP (0.01% IN 1μs) USES HERMETIC TRANSISTORS FOR RELIABILITY

Using hermetically-sealed metal-can semiconductors throughout, the FET-input Model 47 achieves ultra-fast performance over the range from −55°C to +125°C, with specifications guaranteed from −55°C to +85°C. It is available in four models, graded for performance and temperature range. Its high input impedance, fast settling time, low voltage drift and bias current, and small size suggest use as a buffer amplifier, sample-hold amplifier, or for unloading R-2R networks or *MINIDAC's* for high-speed conversion in military or mobile applications. Prices begin at $69. (1–9) for the 47A.

Gain (min)	100,000
Output (min)	±10V, ±10mA
Load Capacitance Range	0 to 1000pF (stable)
Full Power Response (min)	800kHz
Slew Rate (min)	50V/μs
Settling Time (max) Inverting or Non-inverting	1μs to ±0.01%
Offset Voltage Drift (max)	50/15μV/°C
Bias Current (max, +25°C)	50/25pA
Size	1-1/8"x1-1/8"x0.4"

THE AD503 vs...?

by Stan Harris

This issue's cover story introduces the AD503, a new high-performance IC FET-input operational amplifier in the TO-99 package using two chips (a dual FET and a specially-designed complementary op amp). For high performance in a small package at low price, it seems intuitive that, given today's technology, this has to be a winning approach. However, other choices do exist. In this article, we consider briefly the more salient choices available today. (Although the discussion does not embrace Analog's wide choice of encapsulated modular types, the reader should be aware that where size and cost permit, some of today's best specifications are available only in modular FET-input op amps.)

FET OP AMPS, MAKE OR BUY?

Often, the circuit or system engineer considers designing his own FET-input operational amplifier, tempted by the possibilities of saving $10–$20 per op amp, using low cost op amps and dual FET's. Here are a few of the issues he should consider:

1. *Performance vs. complexity.* In general, high performance calls for complex circuits. The resistor-FET-pair-IC op amp circuit shown on page 7 is modest in both complexity and performance. The circuit of Figure 8 (page 8) is better, but it adds resistors and transistors. If "bootstrapping" were added to stabilize V_{DG}, the amplifier's bias current would be constant over the common mode range (and CMRR would be increased), at the cost of perhaps 4 discrete transistors, plus resistors. Finally, a more complex current source would further improve stability. These options require extra parts, a place to put them, money to pay for them, etc. However, it is easy for the IC manufacturer to incorporate all of the above features by designing a modified general-purpose IC amplifier—without adding much silicon "real estate", and thus without greatly increasing cost.

2. *Reliability.* The discrete component circuit, in any form, requires many more circuit board interconnections than the IC device, typically, from 12 to 25 additional solder joints. From the standpoint of reliability, these additional interconnections—plus the fact that the most sensitive parts of the amplifier are exposed to external influences—make the discrete component FET approach inherently less reliable than the integrated hermetically packaged IC.

3. *Ease of manufacture.* The components require assembly into a circuit board. Thus, the component approach adds weight, size, and layout complexity. In addition to the circuit design, component selection, breadboard evaluation, and board layout, the user must consider parts procurement, stock inventory, incoming inspection, assembly cost, shrinkage, etc. In contrast, a well-designed FET-input op amp required one design, needs but one evaluation, one socket, one purchase, one assembly operation, one stock bin and inspection procedure.

4. *Cost.* In its *simplest forms,* the component approach appears less costly than the higher-performance IC, especially if one fails to take into account the less obvious cost factors. The gap closes rapidly with increasing complexity. Moreover, integrated circuits have a history of decreasing prices. Thus, the user who designs the FET IC into his systems now will have a significant performance advantage—as well as competitive cost—when the production phase is reached.

BUYING FET OP AMPS TODAY: AD503 or μA740?

Once the decision is made to buy a FET IC op amp, one must consider what is available. Because monolithic technology appears to offer what will ultimately be the most competitive costs, let us compare Analog's AD503 family with μA740C and μA740, the only purely monolithic FET-input op amps now available. At present, the AD503's prices are quite competitive with those of μA740. However, even if the μA740 prices should drop to zero, the specifications below indicate the limits of available performance.

Parameter	AD503J§	μA740C	AD503K§	μA740
Max V_{OS} (mV)	50	no spec*	20	20
Max I_{OS} (pA)	25	no spec*	10	no spec*
Max I_b (pA)	50	2000	25	200
Max ΔV/ΔT (μV/°C)‡	75	no spec*	25	no spec*
Min Gain (V/V)	20k	no spec*	20k	50k
Max PSRR (μV/V)	no spec*	no spec*	300	300
Min CMRR (dB)	no spec*	no spec*	70	64
Min V_{in} (V)	±10	±10	±10	±10
Min V_O (V)	±10	±10	±10	±10
Min Slew Rate (V/μs)	4†	no spec†	4†	no spec†
Max Supply Current (mA)	5.5	8.0	5.5	5.2

* Parameter given as typical value only

† Typical slew rate: 6V/μs

‡ Much can be gained by an informed analysis of the incremental relationship between offset and drift specifications, based on the manufacturers' published circuit schematics, assuming temperature-stable current sources. (Examination of the μA740 circuit and measurements of both types confirm the calculations.)

For μA740. Each millivolt of offset trim adjustment requires about 0.4% change in drain current, which in turn results in a change in V_{OS} drift of 4μV/°C. Thus, trimming 20mV (μA740) of offset to zero can result in a drift change of 80μV/°C (near +25°C). This change will add to the original drift rate specified. Since that parameter is unspecified, drift determination is left as an exercise for the user. As for μA740C, not even the change due to offset trimming can be determined because maximum initial offset is not specified.

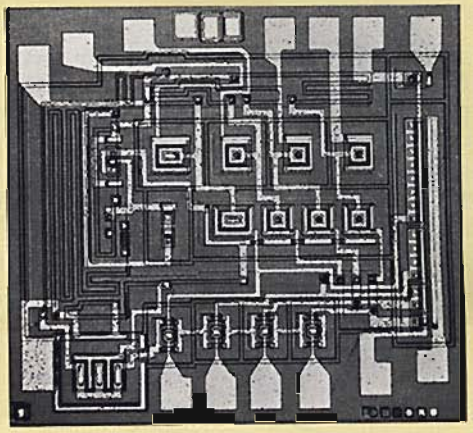
For AD503. Each millivolt of offset, as it is trimmed, produces a change in temperature drift near +25°C of 1/3μV/°C. Thus the change in offset drift caused by trimming out the full amount of offset is 16.7μV/°C maximum for AD503J and 6.7μV/°C for AD503K. These should be added to the specified maximum offset drifts of 75μV/°C and 25μV/°C.

Measured noise in a 50kHz bandwidth for the two families is AD503: 8μV rms; μA740: 25μV rms.

The AD503J and AD503K are hybrid circuits which combine a monolithic dual FET with a specially designed monolithic amplifier chip. This design permits optimization of the characteristics of both the dual-FET and custom monolithic op amp since they are processed independently, thereby allowing selection of the best starting material and doping levels for each device. Thus, the two-chip approach provides higher performance than the single chip technique, in which the FETs are integrated with the bipolar op amp.

§Preliminary specs, will be improved.

HIGH PERFORMANCE μDAC MONOLITHIC IC CONVERSION COMPONENTS



μDAC CONCEPT—μDACs are monolithic IC devices containing four logic operated switches and associated circuitry. When they are connected with precision resistors and reference circuitry, they form 4-, 8- and 12-bit D/A and A/D converters.

Two models are available. The Model AD550, using current switching techniques is recommended where high speed and accuracy are paramount, while the AD555 voltage switch is optimized for applications where both digital and analog signals vary—such as in digital to synchro conversion or multiplying DAC applications.

AD550
FEATURES:

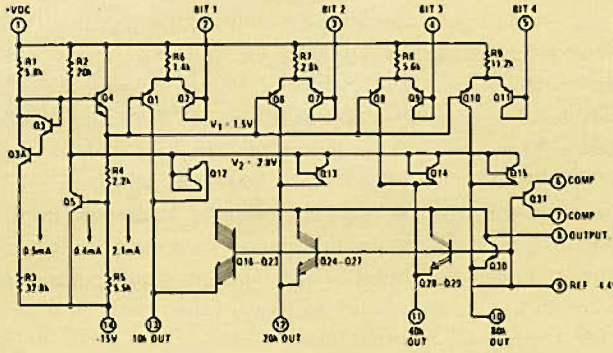
- 12 Bit Accuracy (±½ LSB)
- Low TC ±5ppm/°C, max
- 0.5μsec Switching Speed
- -55°C to +125° Temp. Range
- Hermetic Flatpack or DIL

APPLICATIONS:

- A/D Converters . . . D/A Converters
  - For Display Systems
  - Avionic and Military Systems
  - Computer Interface Systems

AD555
FEATURES:

- Independent Variable Bipolar References
- 25Ω "on" resistance—Less than 10Ω Mismatch
- Less than 2mV offset—Less than 1.0mV Mismatch
- 5ppm/°C Tracking between Switches, max
- TTL, DTL, RTL Compatible
- Hermetic Flatpack and DIL



Schematic Diagram of AD550 Monolithic Quad Switch

MATCHING THIN FILM RESISTORS: The AD850 series monolithic resistor networks complement the monolithic μDAC IC's. These complete networks feature ±1ppm/°C tracking and include all resistors necessary to build a 12-bit D/A converter.

HEARD ABOUT THE μDAC PRICE REDUCTIONS? A substantial price reduction on μDAC IC's has been recently announced. For more information on μDAC's and their prices, contact your local ADI representative.

COMPACT MODULAR ULTRALINEAR 12-BIT A/D CONVERTER 2" X 4" X 0.4"

FEATURES USER WIRED OPTIONS...and retains all the other superb characteristics of the already popular card-mounted ADC-Q; 8-, 10-, or 12-bits, low TC monotonicity, and μDAC IC construction. As a bonus, the various input scaling options can be wired, externally, for the range desired. The internal clock connections are externally available, making it possible to disable the internal clock, and use a system clock. The ADC-QM is completely compatible with our other data acquisition components. Check the features and specs below.

FEATURES:

- 8-, 10-, and 12-Bit Resolutions and Accuracies
- Low Cost/Performance Ratio
- Low (±10ppm/°C) TC
- Externally Wired Options
- Binary or BCD
- Compact (2"x4"x0.4") Module

SPECIFICATIONS:

Relative Accuracy	±½LSB
Differential Linearity	±½LSB
Input Voltage Range	±5V, ±10V, or 0 to +10V
Output Codes	Binary, Offset Binary, 2's Complement, BCD
Power Requirements	±15V, +5V
Price: (1–9)	
ADC-8QM	$250.
ADC-10QM	$280.
ADC-12QM	$305.

NEW PRODUCTS

MONOTONIC 12-BIT D/A CONVERTER IN 2" X 2" X 0.36" MODULE USES μDAC IC'S

DAC-QS FEATURES:

- 8-, 10-, 12-Bit Accuracy
- Compact (2"x2"x0.36")
- Low TC (±7ppm/°C)
- Low Supply Sensitivity (0.002%/%)
- Fast (< 5μsec to 0.01%)

THE DAC-QS—series D/A converter is a compact modular version of the popular card-mounted ultra-linear DAC-Q. Input code is complementary binary, and 4 output voltage ranges are available.

The DAC-QM (2" X 4" X 0.4") is a version of the DAC-QS with input storage registers. Codes for the DAC-QM are Binary, BCD and their complements.

Price (1—9):
DAC- 8QS; $140; DAC-10QS; $170. DAC-12QS; $190.
DAC- 8QM; $170: DAC-10QM; $210: DAC-12QM; $230.

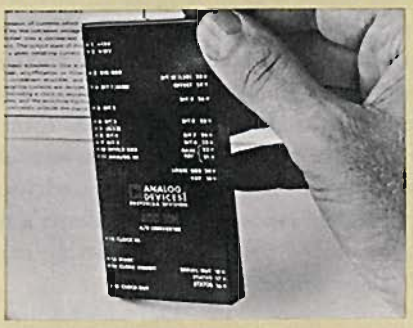
LOW COST-MODULAR A/D CONVERTER

MODEL ADC-8/10H SPECIFICATIONS

Inputs:	
Digital Control Inputs (TTL, DTL Compatible)	"0" < 0.8V @ −1.6mA max "1" > 2.0V @ 40μA max
Analog Input Options	0 to +10V, 0 to +5V 0 to −10V, ±10V, ±5V
Output Signals:	(a) Parallel binary (TTL) (b) Serial binary (TTL)
Accuracy (Including Quantization)	±1 LSB (ADC-8H) ±1 LSB (±0.1% of full scale) (ADC-10H)
Temp. Coefficient:	
Unipolar—zero	±0.025 LSB/°C max
—gain	±50ppm of Reading/°C max
Bipolar —zero	±0.04 LSB/°C max
—gain	±50ppm of Reading/°C max
Temp. Range:	
Operating	0°C to + 70°C
Storage	−55°C to +125°C
Power Supply Req:	+15VDC ±2% @ 40mA max −15VDC ±2% @ 30mA max +5VDC ±5% @ 320mA max
Price: (1—9)	
ADC- 8H	$195.
ADC-10H	$225.
Specify: Optional Input Buffer Amplifier $35. Additional	

FEATURES:

- Low Cost: $195. for ADC-8H
- 10 Bits Resolution in 18μs (±½ LSB)
- Low Profile (0.4") Module
- Serial and Parallel Data Out
- MSB Complement Available
- Fully Monotonic



ADC-8/10H—Are low cost, low profile, modular successive approximation, analog-to-digital converters. These modules are completely self-contained, and include many extras not normally found in a complete A/D converter of such low cost. Output Data is presented in serial and parallel form. Various input voltage options are available, including unipolar or bipolar operation.

The heart of the ADC-10H is the MDA-10H digital-to-analog converter. Also included is a clock, comparator, required logic and optional input buffer op amp where high input impedance is needed. The ADC-8H is similar, but with 8-bits of resolution and having a total conversion time of 15μs.

FOUR-QUADRANT MULTIPLYING DAC'S

FEATURES:

- 4 Quadrant Multiplication
- Up to 12 Bit Resolution
- 3dB Bandwidth: 120kHz
- ±10 Volt Output Capability
- Low Profile—2x2x.4 inches

MODEL DAC-8/12M

Resolution:	8 or 12 bits
Ref. Input Range:	±5V or ±10 Volts (±4V without input amplifiers)
Logic Input:	"0" < 0.8 volts @ −0.5mA max "1" > 2.0 volts @ +0.1mA max
Accuracy:	0.024% of Full Scale for DAC-12M 0.20% of Full Scale for DAC-8M
Maximum Gain:	1.9994
Settling Time:	50μsec (for either axis)
Input Impedance:	5kΩ(±5V), 10kΩ(±10V)
Output Capability:	±5 Volts or ±10 Volts at ±10mA
Temp. Coefficient:	±15ppm/°C
Operating Temp:	0 to +70°C
Power Supply:	+15V at +17mA −15V at −20mA
Price: (1—9)	
DAC- 8M	$195.
DAC-12M	$295.

DAC-M—A four quadrant hybrid multiplying digital-to-analog converter whose output voltage is proportional to the product of digital and analog input signals. The analog signal can be ac, or a varying dc signal. This unique design owes its superb performance to Analog's μDAC, AD555 IC's.

Available options are BCD or binary digital inputs and ±5V or ±10V analog signals.

A Frequency Modulation Detector Using Operational Amplifiers

by Eugene T. Patronis, Jr., School of Physics, Georgia Institute of Technology

Integrated circuits are bringing about extraordinary changes in the electronics industry. These changes are manifested in many ways. The radical differences in the manufacturing processes of integrated circuits as compared with circuits assembled from discrete components are self-evident. In addition, however, there are notable differences in circuit capabilities and in design considerations as well. In general, integrated circuits have a higher circuit density, greater speed, and lower power dissipation when compared with conventional circuits. Integrated circuits lend themselves quite readily to those applications where a large number of circuits of a particular type are required, as in computer circuitry. They are finding increasing use in linear circuits where the applications can be tailored to a few standard configurations. Circuit designers will be called upon more and more in the future to design around a few standard integrated circuits or to evolve circuits which can be totally reduced to the integrated form. An example of a circuit design innovation which allows a frequency modulation detector to be produced completely as an integrated circuit will be given here.

Frequency modulation detectors usually take the form of a limiter-discriminator or ratio detector. Both of these circuits depend in part upon a tuned transformer for their operation. The other components in these circuits, such as transistors, resistors, diodes, and capacitors can all be readily produced in the integrated circuit form. The transformer can be integrated only with extreme difficulty (if at all). A circuit not requiring a transformer or other inductors would allow the detector to be produced completely in the integrated form. Clearly, the transformer must be eliminated. In order to see how this may be accomplished, consider the function that must be performed by the detector:

When the detector is presented with a signal whose frequency is f_o, the output of the detector is to be zero. When the detector is presented with a signal whose frequency is f, the output of the detector is to be a voltage whose value is proportional to Δf where $\Delta f = f - f_o$. In most applications Δf is no greater than one percent of f_o. The fact that the detector output is zero when the input is at a frequency f_o is suggestive of a null or balance technique. That is, if two signals, say A and B, can be derived from the input signal in such a way that their amplitudes are equal at the frequency f_o, then the difference of the magnitudes of these two signals will be zero at the frequency f_o. Furthermore, if the amplitude of A is an increasing function of f while the amplitude of B is a decreasing function of f, then the amplitude of the difference signal A-B contains information about Δf.

Let the input signal to the detector be a constant amplitude sine wave denoted by $e_i = E \sin(2\pi ft)$. From this signal must be derived the two signals A and B. The amplitude of signal A must be an increasing function of f. It is a well-known property of sinusoids that their time derivatives are proportional to f. The amplitude of signal B must be a decreasing function of f. This can be obtained through the time integral of a sinusoid which is inversely proportional to f. The signals A and B can thus be derived from the input signal e_i by the operations of differentiation and integration, respectively. These operations can be performed electronically with great accuracy by means of operational amplifiers, which can be constructed in the form of completely integrated circuits.

Figure 1 depicts a detector circuit arranged according to the considerations just discussed. The triangles represent inverting operational amplifiers having large open loop voltage gains for frequencies in the vicinity of f_o. The generator represents a frequency modulated signal source of the form:

$$e_i = E \sin(2\pi f t).$$

The operational differentiator produces an output signal e_A of the form:

$$e_A = -RC\,2\pi f E \cos(2\pi f t)$$

which, when rectified by the diode D_A and filtered by the network R_L and C_L, become E_A, where:

$$E_A = \eta RC\,2\pi f E,$$

η being the rectification efficiency. The operational integrator yields an output signal e_B of the form:

$$e_B = \frac{E}{RC\,2\pi f} \cos(2\pi f t)$$

which, when rectified by the diode D_B and filtered by the network R_L and C_L, becomes E_B, where:

$$E_B = \frac{-\eta E}{RC\,2\pi f},$$

assuming the same rectification efficiency. The output of the overall detector is then e_o, as given by:

$$e_o = \eta E \left[RC\,2\pi f - \frac{1}{RC\,2\pi f} \right].$$

If now the integration and differentiation time constant RC is chosen so that:

$$RC = \frac{1}{2\pi f_o}$$

Portions of this article appeared in the February 1970 issue of *AUDIO* magazine, a publication of North American Publishing Company

then e_o will become:

$$e_o = \eta E \left[\frac{f}{f_o} - \frac{f_o}{f} \right]$$

Remembering that $f = f_o + \Delta f$, we now have:

$$e_o = \eta E \left[\frac{f_o + \Delta f}{f_o} - \frac{f_o}{f_o + \Delta f} \right]$$

$$= \eta E \left[1 + \frac{\Delta f}{f_o} - 1 + \frac{\Delta f}{f_o} - \frac{\overline{\Delta f}^2}{f_o} + \ldots \right]$$

Now $|\Delta f|$ is much less than f_o, so

$$\left[e_o = \eta E \frac{2\Delta f}{f_o} \right]$$

which is just the desired form.

This detector offers a number of advantages other than the fact that it can be constructed completely in the integrated form. The operational amplifiers provide excellent isolation between the signal source and the detector load. The detector can readily be tuned by varying the time constant RC. In fact, this tuning could be accomplished remotely under voltage control by letting C be furnished by a silicon varactor diode. Finally, this detector can be used for a very wide range of frequencies, f_o.

Two models of the detector have been constructed. One circuit was built from discrete components while the other was built from commercially available operational amplifiers. The first of these has been employed at several frequencies ranging from low audio up to 10.7 megahertz. The latter has been used for frequencies as high as 4.5 megahertz. In the detector application, it is not necessary that the amplifiers have response down to DC; therefore drift problems can be readily corrected by employing suitable high pass filters in either the input or output circuits of the amplifiers. In fact, the circuit built from discrete components was AC coupled internally to avoid this problem. However, both models have been equally successful in the frequency ranges mentioned.

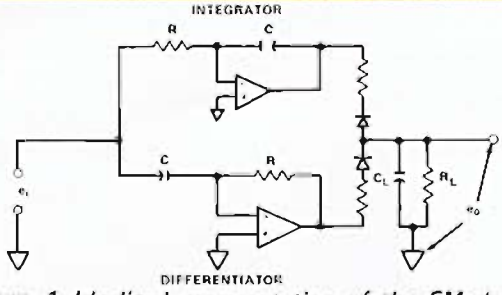


Figure 1. Idealized representation of the FM detector circuit. In practice, to avoid dc drift, the integrator would be ac-coupled through a capacitor much larger than C, and C would be shunted by a feedback resistor much larger than R; the differentiator would have a resistor much smaller than R in series with C, and R would be shunted by a capacitor much smaller than C, for noise reduction and dynamic stability.

Editor's Notes:

Paper Call. We have a gnawing hunger for articles illustrating new and better ways of using analog devices. Our only rule is that the applications be useful, i.e., that they "work", and that a large number of readers could benefit from reading and applying what they read. Other additional virtues, such as brevity, succinctness, and authority, are naturally desirable, but not essential. "Analog Briefs", little morsels with a single cogent idea, are especially welcome. We do not hesitate to award honororia when we print fresh unpublished articles submitted from outside the family.

Comment Call. We have plenty of ideas about what we think should turn you on, but we need your comments to keep us on the right track. Write, and tell us what you like or don't like about this publication, what you'd like us to emphasize or to abandon. Pat us on the back, or beat us on the head, but do let us hear from you. Your feedback helps maintain the *Dialogue*, in the most literal sense.

DAN SHEINGOLD

Readers' Notes:

I have read your excellent article on "Noise and Operational Amplifier Circuits" appearing in the March 1969 issue of *Analog Dialogue*.

I write in regard to the chart (Figure 14, page 14) showing voltage and current noise of your Model 230 Chopper-Stabilized Amplifier. In this data, voltage noise is shown extrapolated as a constant value ($2\mu V/\sqrt{Hz}$) down to 0.01Hz.

If this holds true, it implies that Chopper-Stabilized Amplifiers have the ability to eliminate pink (1/f) noise.

Would you please comment on this point.

C. L. Pomernacki
University of California
Livermore, California

The extrapolation is valid for the field of the chart, but not necessarily at lower frequencies.

The gain of the chopper amplifier reduces, but does not eliminate, 1/f noise. The chopper amplifier can be thought of as an integrator, i.e., its response increases with decreasing frequency, until the dc-open-loop gain of the chopper amplifier is reached; then it levels off. Below the frequency at which the gain becomes constant, if 1/f noise is still present in the amplifier, the overall noise will again start increasing, probably following the trend indicated between 1kHz and 10Hz, reduced by the open-loop chopper gain.

At such low frequencies, it is hard to get adequate measured data, because of the need for a large number of integrations over long periods. Furthermore, 1/f noise can be masked by long term drift, thermal offsets, etc.

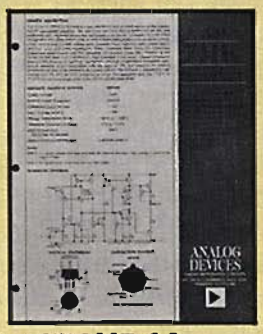
FREE!

16 NEW PUBLICATIONS FROM ANALOG DEVICES, INC.

These data sheets and application notes have appeared since the June 1970 issue of *Analog Dialogue*. They are available at no charge. If there are any that you want, just circle their numbers on the reply card, and we'll mail them out to you immediately.

If your interest is more immediate, and you'd like to buy, try, or chat about an application, just phone Analog Devices, or the nearest sales office.

1. NEW MULTIPLIERS FAST, LINEAR, ACCURATE



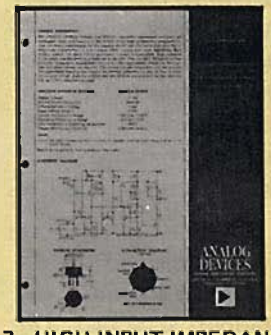
2. LOW COST, G.P. IC OP AMPS AD741 FAMILY

3. NON-INVERTING 0.1μV/°C CHOPPER OP AMPS

4. ULTRA-FAST D/A CONVERTERS 50ns RESPONSE

5. MONOLITHIC μDAC VOLTAGE SWITCHES FOR 12-BIT D/A'S

6. POWER OPERATIONAL AMPLIFIERS TO 1kW

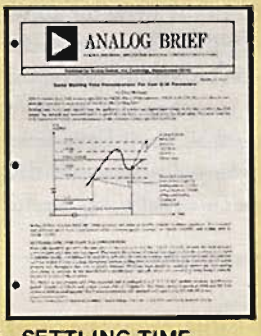


7. HIGH INPUT IMPEDANCE MONOLITHIC OP AMPS

8. ULTRALINEAR A/D & D/A CONVERTERS TO 12 BITS

9. DESIGNING WITH μDAC MONOLITHIC D/A SWITCHES

10. TWO HIGH PERFORMANCE 0.01% SAMPLE-HOLDS

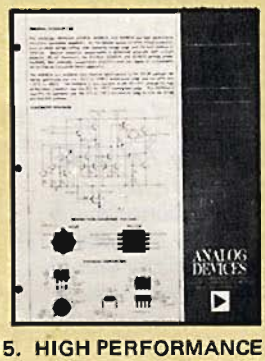


11. SETTLING TIME VS. ACCURACY IN DAC'S

12. NEW LOW COST CHOPPER STABILIZED OP AMPS—0.1μV/°C

13. NEW LOW COST A/D CONVERTER 8 & 10 BITS

14. SERVO MULTIPLICATION WITH MULTIPLYING DAC'S



15. HIGH PERFORMANCE MONOLITHIC OP AMPS AD101 FAMILY

16. ULTRA LOW BIAS CURRENT FET-INPUT OP AMP 0.15pA